## REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Office Action of September 20, 2005, which has been made FINAL, the Examiner finally rejected Claims 1-4, 14-18 and 20-23 under 35 U.S.C. §102(e), as being allegedly anticipated by Funaba (U.S. Patent No. 6,853,213) (hereinafter "Funaba").

The Examiner did indicate that Claims 5-13, 19 and 24 presented allowable subject matter if rewritten in independent form including all of the limitation of the base claim and any intervening claims.

Applicants respectfully requests entry of these remarks as they are intended to further clarify, with exemplary Exhibits attached hereto, the operation of the invention and highlight the distinctions over the cited prior art reference. This response additionally addresses the Examiner's Response to Arguments and hence, could not have been earlier presented.

With respect to the rejection of Claims 1-4, 14-18 and 20-23 under 35 U.S.C. §102(e), as being allegedly unpatentable over Funaba, applicant respectfully disagrees.

With respect to the rejection of Claims 1-4, 14-18, and 20-23, the Examiner took to task in the Response to Arguments section (page 4, ¶ 4 of the Final Rejection), the remarks and arguments presented in applicants prior response of July 8, 2005 in response to the first Office Action of April 13, 2005.

With respect to the applicants prior remarks, the Examiner states that Kuroda (US 5,742,183) (hereinafter "Kuroda") allegedly presents a teaching that a resistor could be

considered a current source as shown in Figure 11A of Kuroda. The Examiner specifically relies on Kuroda as allegedly teaching that a p-type MOSFET when fully on or in linear mode behaves "like a current source since the current is carry[sic] through the transistor like a resistor..". Based on this reasoning, the Examiner thus alleges that in Funaba, the combination of MP11 and R11 in Figure 1A of Funaba is considered a current source when MP11 is fully turned on or in a linear mode.

Applicants respectfully disagree and respectfully submit the following:

It appears that the Examiner is relying on recitation in Kuroda at column 8, lines 27 to line 34 and Figs. 11A, 11B and 11C of Kuroda which allegedly depicts a resistor used as a current source, i.e., a FET with a fixed gate voltage is a current source. Therefore the Examiner makes the argument that the circuit in Fig. 1A of Funaba, MP11-R11, MP12-R13, MN11-R12, MN12-R14 form a current source. Respectfully, the sourcing and sinking current sources as claimed in independent Claims 1, 14 and 20 of the present invention are not taught by the alleged current source as Examiner states is allegedly taught by the combination of Funaba in view of Kuroda.

1) First of all, Kuroda is directed to a level shifting device for coupling signals from one circuit to a connected circuit having differing voltage supplies; thus the statements of column 8, line 27 to line 34 and Figs. 11A, 11B and 11C of Kuroda are not applicable to the present disclosure.

2) The definition of a current source, e.g., as found in a book entitled "Circuit And Signals: an Introduction To Linear And Interface Circuits" by Roland E. Thomas and Albert J. Rosa, state that "the current source supplies Is, amperes out of its + terminal and into its – terminal, and will furnish whatever voltage is required by the circuit to which it is

connected". It is very obvious and clear that a current source can supply a current independently from the voltage applied on it. A copy of page 24 of the aforementioned book providing this teaching is attached hereto as exhibit A for the Examiner's convenience.

3) Ohm's Law ($I = \frac{V}{R}$) indicates that when the voltage across the resistor R changes, the current will change linearly, i.e., it can not be constant. Therefore a resistor is not a current source. In the integrated circuits, usually the power supply range e.g., 3.5 V - 5V is widely used, and a power supply variation may be about 10%. Thus, the current range is about several tens of uA to a few mA. Thus, as shown in Funaba, resistors R11, R12, R13, R14 are used for transmission, their resistance is 50 ohms, when an example power supply voltage of 5V changes 10%, the current change on these resistors is 10mA. Therefore, it is respectfully submitted that these resistors are never a current source.

4) P-type FET or an N-type FET with a fixed gate voltage are not always a current source. Applicants respectfully attach, in an exhibit B, two pages of a book entitled "Principles of CMOS VLSI Design"2nd edition by Neil H.E. Weste that is directed to CMOS technology. These attached passages provides describe (in section 2.2.1) Basic DC Equations" marked as Exhibits B1 and B2, which show that

1) Only when 0<Vgs-Vt<Vds where Vgs is the voltage of the gate to source, Vt is the threshold voltage of the FET, the FET is in the saturation region or saturation mode, i.e., the current of Ids is independent of the voltage Vds, and thus, the FET behaves as a current source [see the formula in equation 2.5c in reference page labeled B2]; and,

2) Other two operation regions:

   A cutoff region: Ids=0 when Vgs =0 [see the formula in equation 2.5a in reference page labeled B1]. This mode of operation does not constitute a current source.

A linear region: Ids is dependent of Vds [see the formula in equation 2.5b in reference page labeled B1]. This mode of operation does not constitute a current source.

5) Respectfully, in all the figures of Funaba, the gates of MP11, MP12, MN11, MN12 are connected to the outputs of a digital circuits (either a high level "1" or a low level "0"), the gate voltages of the FETs are VDDQ or 0V. When Vg=0, the PFETs (MP11 and MP12) are operable in the linear region, the NFETs are at cutoff region, when Vg = VDDQ, the PFETs are at cutoff region, the NFETs are at a linear region, so that the FETs are switching between the cutoff region and linear region, they never operate in the saturation region. Therefore, they never perform as current sources.

Moreover, it is respectfully submitted that Figure 2 of the present invention, to which independent Claims 1, 14 and 20 are directed, provides a driver structure that comprises a switching current source in parallel with a fixed resistor, a switch current source and a fixed resistor are difference elements, and the fixed resistor plays an important role in the low reflection performance, particularly, by avoiding the instant high impedance at switch transition. Contrarily, as shown in Fig.1A of Funaba, the parallel elements: MP11-R11 and MP12-R13, MN11 and MN12 are identical, there is no fixed resistor, there is no switching current source leading to the beneficial behavior of the present invention as claimed in independent claims 1, 14 and 20.

Thus it is respectfully submitted that the cited Funaba reference whether taken alone or in combination with Kuroda can not cover the disclosure. That is, Funaba, whether taken alone or in combination with Kuroda, does not teach or suggest a low reflection driver for a high speed simultaneous bi-directional transmission line/data bus which is designed such that units at both ends of the transmission line/data bus there is configured a switching current

source connected to a matching resistor in parallel. According to the invention, as the impedance of the switch current source is always much larger than the resistance of matching resistor regardless of whether the main MOSFETs providing the switching currents are in saturation mode or in cut-off mode, the resultant resistance is always equal to the resistance of the matching resistor.

Being the case, the Examiner's interpretation of the device in Funaba relied upon in his rejection of independent Claims 1, 14 and 20 is misplaced. Moreover, in the Response to Arguments section, the Examiner's indication that MP11 is connected "in parallel to R13" appears misplaced, not the least because MP11 of Funabe Figure 1A is **not a current source** (i.e., in Funaba, the INV (inverter circuit) output voltage is only one of two values: 0V or VDDQ and thus will render MP11 in either linear mode and its behavior is like a resistor; or in cut-off mode and the behavior is like an open circuit) and further because it is the series connection of MP11 and R11 that is "in parallel" with a circuit "finger" comprising the series connection of MP12 and R13 which functions in a manner different from the present invention and is a different circuit altogether being that MP11 and MP12 are not operable current sources in Funaba.

In view of the foregoing distinction provided herein, the Examiner is respectfully requested to withdraw the rejection of Claims 1, 14 and 20 and all claims dependent thereon.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition

of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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SF:gc
Attachments: Exhibit A
Exhibit B

# EXHIBIT A

A



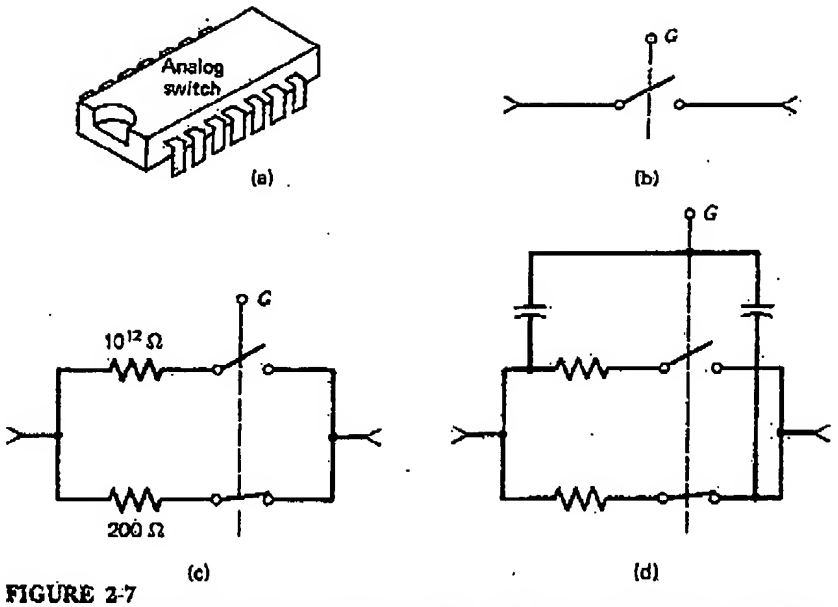


**FIGURE 2-7**
**The analog switch. (*a*) Actual device. (*b*) Basic model. (*c*) Intermediate model. (*d*) Advanced model.**

Electronic circuits require power to operate. In electronics, there are two types of power sources: voltage sources and current sources. In addition, each of these sources can be either constant, non-time-varying, or time-varying signal sources. The circuit symbols and the $i$-$v$ characteristics of each of these four sources are shown in Figure 2-8. It is noted that there is no separate symbol for a constant current source, whereas there is a symbol for a constant voltage source (a battery). It should also be noted that while the constant voltage source can be only just that, the signal voltage source symbol can also be used to indicate a constant voltage source.

The element equations for the current source are

$$i = i_s \qquad v = \text{depends} \tag{2-10}$$

In words, the current source supplies $i_s$ amperes out of its + terminal and into its − terminal, and will furnish whatever voltage is required by the circuit to which it is connected. The signal voltage source is described by

$$v = v_s \qquad i = \text{depends} \tag{2-11}$$

This means that the voltage source produces $v_s$ volts across its terminals

# EXHIBIT B

B 1



### 2.1.4 Body Effect

As we have seen so far, all devices comprising an MOS device are made on a common substrate. As a result, the substrate voltage of all devices is normally equal. (In some analog circuits this may not be true.) However, in arranging the devices to form gating functions it might be necessary to connect several devices in series as shown in Fig. 2.7 (for example, the NAND gate shown in Fig. 1.6). This may result in an increase in source-to-substrate voltage as we proceed vertically along the series chain ($V_{sb1} = 0$, $V_{sb2} \neq 0$).

Under normal conditions—that is, when $V_{gs} > V_t$—the depletion-layer width remains constant and charge carriers are pulled into the channel from the source. However, as the substrate bias $V_{sb}$ ($V_{source} - V_{substrate}$) is increased, the width of the channel-substrate depletion layer also increases, resulting in an increase in the density of the trapped carriers in the depletion layer. For charge neutrality to hold, the channel charge must decrease. The resultant effect is that the substrate voltage, $V_{sb}$, adds to the channel-substrate junction potential. This increases the gate-channel voltage drop. The overall effect is an increase in the threshold voltage, $V_t$ ($V_{t2} > V_{t1}$).

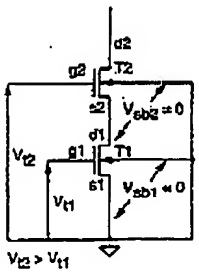


**FIGURE 2.7**
The effect of substrate bias on series-connected n-transistors

## 2.2 MOS Device Design Equations

### 2.2.1 Basic DC Equations

As stated previously, MOS transistors have three regions of operation:

- Cutoff or subthreshold region.
- Nonsaturation or linear region.
- Saturation region.

The ideal (first order, Shockley) equations[6,7,8] describing the behavior of an nMOS device in the three regions are:

*The cutoff region:*

$$I_{ds} = 0 \qquad V_{gs} \leq V_t \tag{2.5a}$$

*The nonsaturation, linear, or triode region:*

$$I_{ds} = \beta\left[(V_{gs} - V_t)\,V_{ds} - \frac{V_{ds}^2}{2}\right] \qquad 0 < V_{ds} < V_{gs} - V_t \tag{2.5b}$$

[Although this region is commonly called the linear region, $I_{ds}$ varies linearly with $V_{gs}$ and $V_{ds}$ when the quadratic term $V_{ds}^2/2$ is very small (i.e., $V_{ds} \ll V_{gs} - V_t$).]

B-2



*The saturation region:*

$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2} \qquad 0 < V_{gs} - V_t < V_{ds} \tag{2.5c}$$

where $I_{ds}$ is the drain-to-source current, $V_{gs}$ is the gate-to-source voltage, $V_t$ is the device threshold, and $\beta$ is the MOS transistor gain factor. The last factor is dependent on both the process parameters and the device geometry, and is given by

$$\beta = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right) \tag{2.6}$$

where $\mu$ is the effective surface mobility of the carriers in the channel, $\varepsilon$ is the permittivity of the gate insulator, $t_{ox}$ is the thickness of the gate insulator, $W$ is the width of the channel, and $L$ is the length of the channel. The gain factor $\beta$ thus consists of a process dependent factor $\mu\varepsilon/t_{ox}$, which contains all the process terms that account for such factors as doping density and gate-oxide thickness and a geometry dependent term $(W/L)$, which depends on the actual layout dimensions of the device. The process dependent factor is sometimes written as $\mu C_{ox}$, where $C_{ox} = \varepsilon/t_{ox}$ is the gate oxide capacitance. The geometric terms in Eq. (2.6) are illustrated in Fig. 2.8 in relation to the physical MOS structure.

The voltage-current characteristics of the n- and p-transistors in the nonsaturated and saturated regions are represented in Fig. 2.9 (with the SPICE circuit for obtaining these characteristics for an n-transistor). Note that we use the absolute value of the voltages concerned to plot the characteristics of the p- and n-transistors on the same axes. The boundary between the linear and saturation regions corresponds to the condition $|V_{ds}| = |V_{gs} - V_t|$ and appears as a dashed line in Fig. 2.9. The drain voltage at which the device

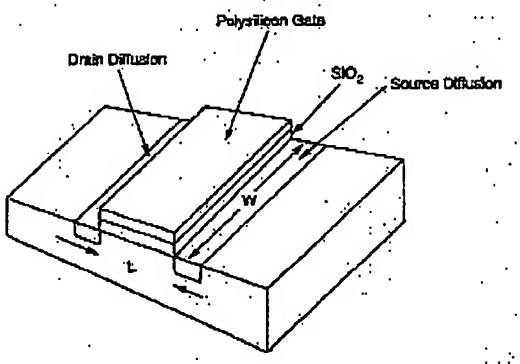


**FIGURE 2.8** Geometric terms in the MOS device equation